2823

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#11 IDS 6-25-03 returned

In re patent application of

Nakagawa

Serial No.: 09/688,203 Group Art Unit: 2823

Filing Date: October 16, 2000 Examiner: William M. Brewster

For: METHOD OF MANUFACTURING SEMICONDUCTOR MEMORY DEVICE

Honorable Commissioner of Patents
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Under the provisions of 37 CFR §1.97 through §1.99 and pursuant to applicant's duty of disclosure under 37 CFR §1.56, applicant respectfully brings the following documents cited in the Japanese Office Action and listed on the attached form PTO-1449, to the attention of the Examiner in charge of the above-identified application. Copies of the listed documents, along with English Abstracts attached thereto, are provided herewith for the convenience of the Examiner.

In compliance with the requirements of 37 CFR §1.98(a)(3), as a concise statement of relevance, as it is presently understood by the individual designated in 35 U.S.C. §1.56(c) most knowledgeable about the content of the information, the undersigned attorney of record submits a translation of portions of an official action by a foreign examiner in which the references were cited. The relevance to the pending U.S. patent application is that the references were cited in a foreign patent application on the same subject matter. However, no independent analysis of the references, the accuracy of the statement of the foreign examiner or the claims of the foreign application under the laws of that country or the United States relative to the subject matter claimed in the present application has been made, the present understanding of the contents thereof by the undersigned being used on the translation of the foreign examiner's comments submitted herewith.

This citation does not constitute an admission that the references are relevant or material to the claims. They are only cited as constituting related art of which the applicant is aware.

I hereby certify that each item of information contained in this Information Disclosure Statement was the first citation of that item by a foreign patent office in a counterpart foreign application, which occurred not more than three months prior to the filing of this statement.

It is respectfully requested that the listed references be considered by the Examiner and formally made of record in this application.

Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-0481.

Respectfully submitted,

Frederick E. Cooperrider
Registration No. 36,769

Date: 6/11/03

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INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

JUN 11 2003 PATENT & TRADEMARK OFFICE

ATTY DOCKET NO.	SERIAL NO.
NEC00P264-ks	09/688,203
APPLICANT(S)	
Nakagawa	
FILING DATE	GROUP
October 16, 2000	2823

RECEIVED JUN 13 2003 TECHNOLOGY CENTER 2800

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
		08-148658	06/07/96	JAPAN			ABS	
		02-151073	06/11/90	JAPAN			ABS	
		10-326881	12/08/98	JAPAN			ABS	
		08-046159	02/16/96	JAPAN			ABS	
		11-233652	08/27/99	JAPAN			ABS	

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

			Japanese Office Action dated March 12, 2003 with partial English translation.

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

WAK.068

Claims 1 to 3 and 5 to 7
Reason 1 or 2

Citation 1

[Remarks]

Particular reference is made to Sections [0061] to [0066] and Figs. 2 to 7.

Claim 1
Reason 3

[Remarks]

Claim 1 states that "the surface of the substrate immediately above the channel region of the select transistor produced in the same process as the central transistor is exposed." However, the substrate itself is not formed in the production process of the transistor. Thus, the description makes the invention unclear. (What part of the select transistor and what part of the central transistor are formed in the same process should be clarified.)

Claims 4 and 8
Reason 2

[Remarks]

Citation 2 discloses a technique to simultaneously form the gate insulating film of a selective transistor of EEPROM and the gate insulating film of high pressure resistance transistor of peripheral circuits. This technique could be readily applied to the invention described in Citation 1 by one skilled in the Art.

It should be noted that amendment should be made for matters that can be derived directly and uniquely from the descriptions of the initially filed Specification and Drawings of the application. For each amendment, a lawful reason for amendment and the corresponding description in the initially filed Specification forming the grounds for the reason should be provided in the Opinion Document.

For the format of Opinion, see the format of Correction Request for Patent Opposition Notice.

Reference Citation List

1. Japanese Laid-Open Patent Application H08-148658
2. Japanese Laid-Open Patent Application H02-151073

Record of the Examination Results relating to Documents of the Prior Art

- Examined Technical Field IPC 7th Edition H01L29/788

  H01L29/792
  H01L27/115
  H01L21/8247

- Documents of the Prior Art

Japanese Laid-Open Patent Application H10-326881
Japanese Laid-Open Patent Application H08-46159
Japanese Laid-Open Patent Application H11-233652

The record of the examination results relating to documents of the prior art do not constitute the grounds for rejection